67-GHz Static Frequency Divider Using 0.2-μm Self-Aligned SiGe HBTs

Katsuyoshi Washio, *Member, IEEE*, Reiko Hayami, Eiji Ohue, Katsuya Oda, Masamichi Tanabe, Hiromi Shimamoto, and Masao Kondo

***Abstract*—A 67-GHz 1/4 static frequency divider using 0.2-μm self-aligned selective-epitaxial-growth SiGe heterojunction bipolar transistors, with a 122-GHz cutoff frequency, a 163-GHz maximum oscillation frequency, and an average emitter coupled logic gate delay time of 5.65 ps, was developed. The pretracking master–slave toggle flip-flop (MS–TFF) of the divider increases the maximum operating frequency to about 15% higher than that of a conventional MS–TFF, yet the power consumption of the divider is 175 mW, which is 1/5 that of comparable dividers, at a supply voltage of −5.2 V.**

***Index Terms*—Bipolar transistors, emitter coupled logic, epitaxial growth, frequency conversion, heterojunctions, millimeter-wave bipolar integrated circuits, MIMICs, optical communication.**

I. Introduction

FUTURE optical communication systems operating at over 10 Gb/s and microwave/millimeter-wave systems for mobile and wireless communication will require high-speed transistor technology. In particular, to meet explosively growing demands for wide-bandwidth radio communications systems, there have been rapid advances in development of monolithic millimeter-wave integrated circuits (MMWICs). The high-speed frequency divider (FD) is a key circuit for applications that require frequency division. Accordingly, given the demand for high-speed, static, and/or quasi-static FD integrated circuits (ICs) operating at frequencies of over 60 GHz, up to 66 GHz with InAlAs/InGaAs heterojunction bipolar transistors (HBTs) [1] and 20–72 GHz with InP/InGaAs HBTs [2] have been developed. However, over the last decade, FD ICs have been mainly based on III–V compound semiconductor devices. To penetrate millimeter-wave systems into the field of consumer electronics, low-cost monolithic ICs are essential for their availability and ease of use.

A SiGe-base HBT with a below-10-ps emitter coupled logic (ECL) gate delay [3], [4] and a cutoff frequency of over 100 GHz [5] is one of the most promising candidates to meet this requirement. We have, therefore, developed a 1/4 static FD fabricated by using 0.2-μm self-aligned selective-epitaxial-growth (SEG) SiGe HBTs with shallow-trench and dual-deep-trench isolations and Ti–salicide electrodes [6], [7]. This HBT was fabricated on a 200-mm wafer line, and the fabrication process is almost completely compatible with 0.2-μm bipolar-CMOS technology [8]. The SiGe HBT exhibited a peak cutoff frequency of 122 GHz, a peak maximum oscillation frequency of 163 GHz, and an average ECL gate delay time of 5.65 ps. The static FD applying the circuit of a pretracking master–slave toggle flip-flop (PT MS-TFF) operated at up to 67 GHz. This toggle flip-flop (TFF) increases the maximum operating frequency to about 15% higher than that of a conventional MS-TFF.

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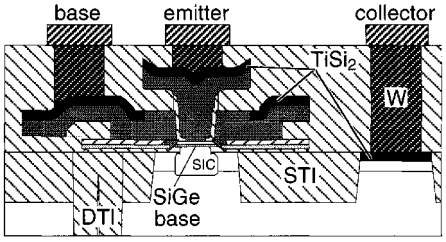

Fig. 1. Schematic cross section of a 0.2-μm SiGe HBT with shallow-trench (STI) and dual-deep-trench (DTI) isolations and Ti–salicide electrodes.

II. Device Structure and Transistor Characteristics

A schematic cross section of the self-aligned SEG SiGe HBT is shown in Fig. 1. An Si-cap/SiGe-base multilayer self-aligned to the emitter was selectively grown. To provide a good link between the intrinsic and extrinsic bases, a poly-Si-assisted self-aligned SEG (PASS) structure was applied [3], [9]. This self-aligned active-region structure provides both low collector capacitance and low base resistance. Furthermore, to reduce the parasitic capacitances of the collector and substrate, respectively, shallow-trench (STI) and dual 0.6-μm-wide deep-trench (DTI) isolations were used. To reduce the parasitic resistance of all electrodes, Ti-salicide layers with a sheet resistance of 3 $\Omega/\square$ were formed. A double selective phosphorus-implanted collector (SIC) in the 0.3-μm-thick Si epitaxial layer and in the undoped SiGe increased the collector–doping level to about 7×10^{17} cm^{-3}.

The 0.6-μm-wide Si-cap/SiGe–base multilayer self-aligned to the 0.2-μm-wide emitter was selectively grown by ultrahigh vacuum/chemical vapor deposition (UHV/CVD) using Si_2H_6, GeH_4, and B_2H_6 source gases at 550 °C for the SiGe layer and Si_2H_6 at 580 °C for the Si layer. The SEG layer consisted of a 20-nm-thick Si cap, 15-nm-thick dual-graded Ge-profile (graded from 0% to 10% and from 10% to 15%) $Si_{1-x}Ge_x$, 40-nm-thick $Si_{0.85}Ge_{0.15}$, and 10-nm-thick Ge-retrograded $Si_{1-x}Ge_x$. A 15-nm-thick 2×10^{19}-cm^{-3} boron-doped $Si_{1-x}Ge_x$ layer was formed as the intrinsic base in the SEG layer.

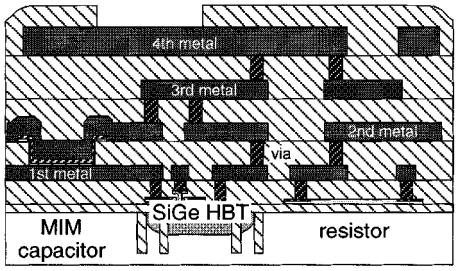

Fig. 2. Schematic cross section of a four-level metal layer structure with an MIM capacitor and a poly-Si resistor.

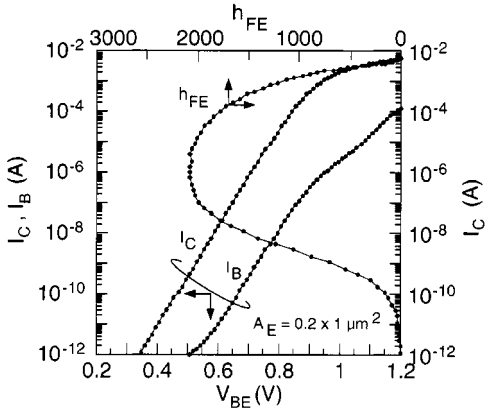

Fig. 3. Gummel plot and current gain $h_{\rm FE}$ dependence on collector current I_C of an SiGe HBT with an emitter area of 0.2 × 1 μm^2.

A schematic cross section of a four-level metal layer structure with a metal–insulator–metal (MIM) capacitor and a poly-Si resistor is shown in Fig. 2. Chemical mechanical polishing was used to planarize the W of the 0.5-μm-wide contact plugs and 0.6 × 0.6-μm via holes and the plasma SiO_2 interlayer insulator. A resistor with a sheet resistance of 220 $\Omega/\square$ was formed by using 200-nm-thick poly-Si. An MIM capacitor with a capacitance of 0.7 fF/m^2 was formed between the first- and second-level metals by using 50-nm-thick plasma SiO_2 as an insulator. The fourth-level (1.35-μm-thick Al) metal provides a high-Q inductor. The process (except the SEG) to fabricate the SiGe HBTs is almost the same as the 0.2-μm bipolar-CMOS process.

SiGe HBTs with an emitter area of 0.2 × 1 μm^2 exhibited good I–V performance with a high peak current gain $h_{\rm FE}$ of 2100, as shown in the Gummel plot, and by the $h_{\rm FE}$ dependence on collector current I_C in Fig. 3. The base–recombination current was below 10 pA, and the current gain was higher than 1000 in the low collector–current region up to 3 nA.

The dependences of cutoff frequency (f_T) and maximum oscillation frequency ($f_{\rm max}$) of the transistors on collector current, whose emitter area was 0.2 × 2 μm^2, at a collector-to-emitter bias voltage of 2 V are shown in Fig. 4. The peak cutoff frequency f_T is 122 GHz and the maximum oscillation frequency $f_{\rm max}$ is 163 GHz. The frequency dependence of the magnitude of h_{21}, maximum stable gain (MSG)/maximum available gain (MAG), and unilateral gain U at I_C of 3 mA is shown in Fig. 5. We attribute this high $f_{\rm max}$ to the high f_T arising from the shallow SiGe base, low base resistance, and low collector capacitance.

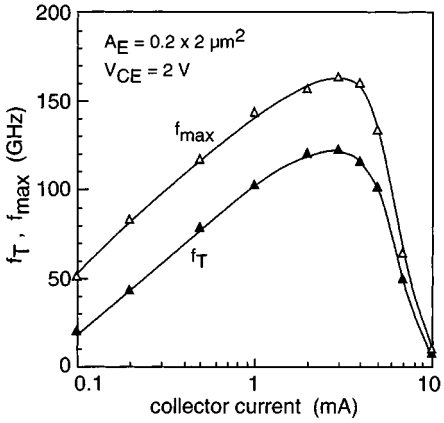

Fig. 4. Cutoff frequency (f_T) and maximum oscillation frequency ($f_{\rm max}$) of an SiGe HBT with an emitter area of 0.2 × 2 μm^2.

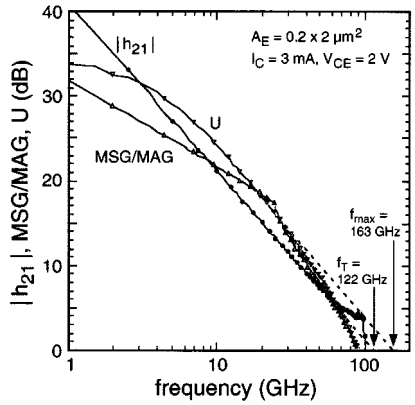

Fig. 5. Frequency dependence of the magnitude of h_{21}, maximum stable gain (MSG)/maximum available gain (MAG), and unilateral gain U for an SiGe HBT with an emitter area of 0.2 × 2 μm^2 at a collector current of 3 mA.

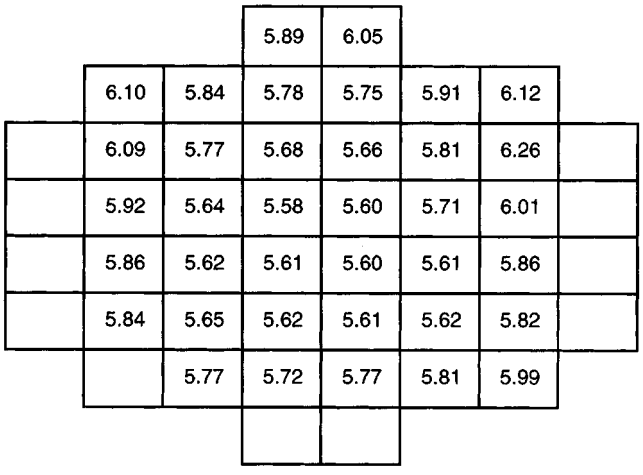

Fig. 6. Map of gate delay time measured by using 53-stage differential ECL ring oscillators at a switching current of about 1.85 mA and a single-ended voltage swing of 250 mV on 200-mm wafer image. An ECL gate delay time is shown in picoseconds. Some positions (blank spaces) were not probed because the probing station could only probe a wafer of less than 150-mm diameter.

The map of gate delay time, measured by using 53-stage differential ECL ring oscillators at a switching current of about 1.85 mA and a single-ended voltage swing of 250 mV, is shown on the 200-mm wafer image in Fig. 6. The average ECL gate

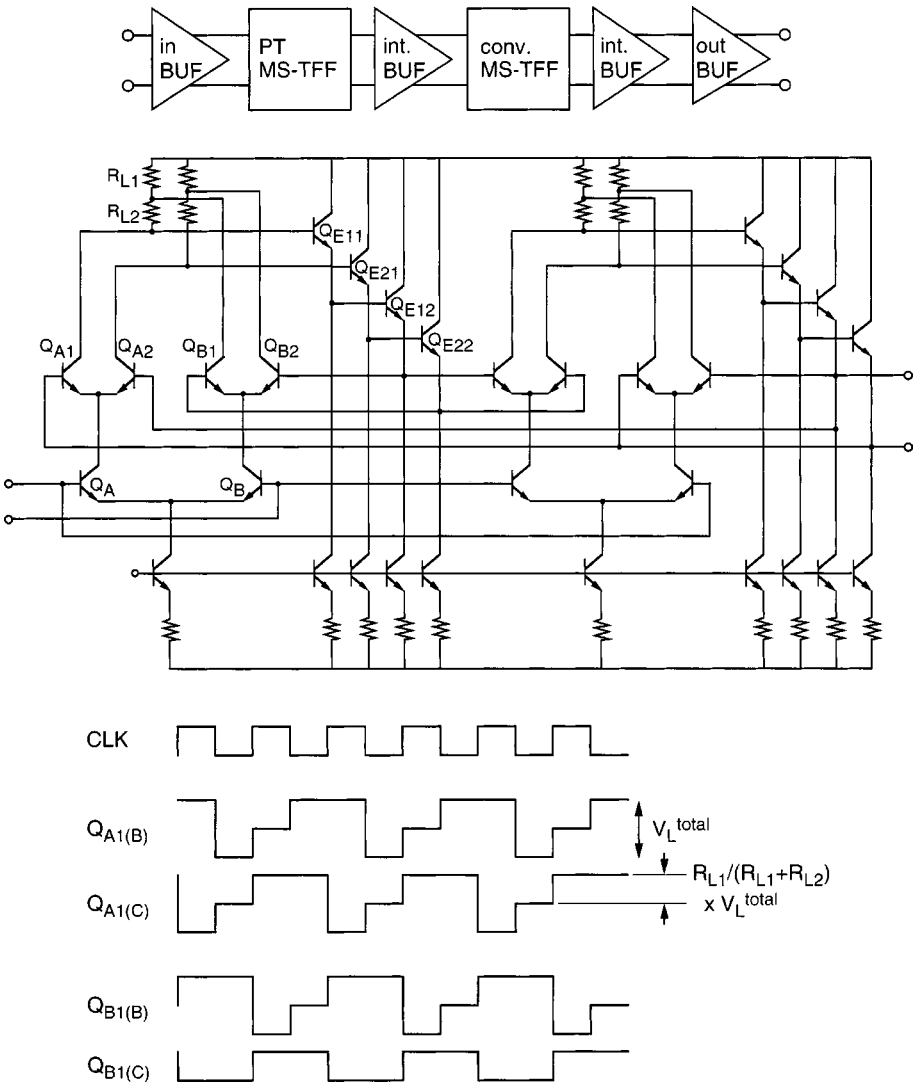

Fig. 7. Block diagram of 1/4 SFD, PT MS-TFF circuit, and operating waveform. B and C in bracket denotes a terminal of base and collector of each transistor.

delay time is 5.65 ps and its standard deviation is 0.96 ps. This ultrahigh-speed operation also indicates the suitability of this SiGe HBT to MMWICs.

III. Static-Frequency-Divider Circuit

A block diagram of a 1/4 static frequency divider (SFD) and the circuit of a PT MS–TFF are shown in Fig. 7. The divider consists of a 50-Ω-terminated three-emitter-follower input buffer, a PT MS-TFF based on a fast comparator technique [10] as the first divide-by-two stage, a conventional master–slave toggle flip-flop (MS-TFF) as the second divide-by-two stage, internal buffers to reform the output signal of each MS-TFF, and an output buffer driving 50-Ω lines. In the PT MS-TFF, to extend the operating frequency, a load resistor was separated into two resistors R_{L1} and R_{L2}, and collector nodes of latching pair transistors were connected at the node between the two resistors. Therefore, the low level of output of the tracking pair rises to a level equal to the product of the PT ratio $(R_{L1}/(R_{L1}+R_{L2}))$ and the total logic swing voltage $V_L^{\rm total}$ during the latching phase. Also, the logic swing voltage of the latching pair is reduced to the same level. As a result, the response of the collector and base nodes of the upper quadrant multiplier becomes faster and, hence, the latch-to-track transition time reduces. We optimized the internal single-ended voltage swing for the MS-TFF to 250 mV by calculating the gate delay time of a single flip-flop biased to operate as an inverter, and typical $V_L^{\rm total}$ of the PT MS-TFF was also set as the same value. To obtain higher operating speed, two emitter followers were used in each stage after the flip-flops. The emitter lengths of each emitter follower transistor were optimized to 1.5 and 3 μm in the master stage and 1.5 and 4 μm in the slave stage to reduce the loading of the flip-flops.

IV. Experimental Results

The input sensitivities of 1/4 pretracking static frequency dividers (PT-SFDs) with different pretracking (PT) ratios compared to those of conventional SFDs at switching currents ($I_{\rm CS}$) of 1.02 and 1.28 mA are shown, respectively, in Fig. 8(a) and (b). The SFDs were measured on-wafer by using 67-GHz microcoaxial probes. The sinusoidal clock input was single-ended driven and the second differential input was terminated at 50 Ω. The dependence of maximum operating frequency $f_{\rm toggle}^{\rm max}$

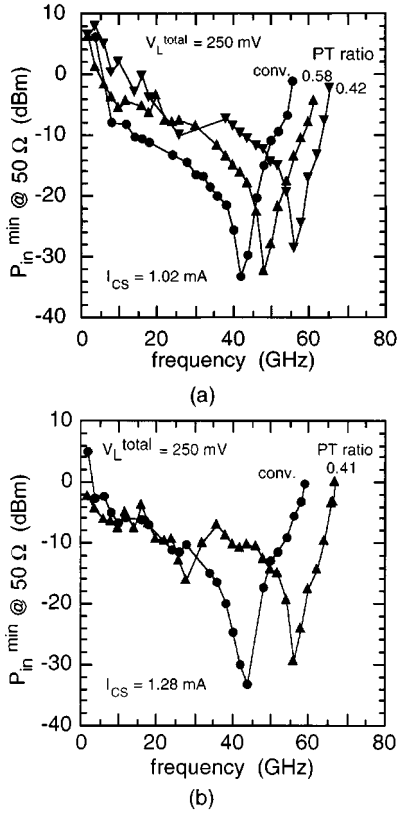

Fig. 8. Input sensitivities of the PT-SFDs with different PT ratios at switching currents ($I_{\rm CS}$) of: (a) 1.02 and (b) 1.28 mA.

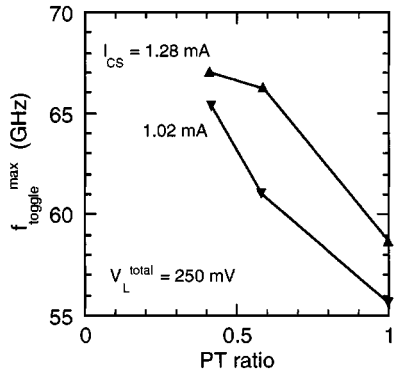

Fig. 9. Dependence of maximum operating frequency $f_{\rm toggle}^{\rm max}$ on PT ratio at switching currents ($I_{\rm CS}$) of 1.02 and 1.28 mA.

on the PT ratio is shown in Fig. 9. The PT-SFD with a PT ratio of about 0.6 operates about 10% faster than the conventional SFD (PT ratio is equal to one), and that with a PT ratio of about 0.4 operates about 17% and 14% faster at $I_{\rm CS}$ of 1.02 and 1.28 mA, respectively. This result indicates that the PT MS-TFF is more effective at the low-power operation because time constants of the collector and base nodes of the upper quadrant multiplier has a strong influence on $f_{\rm toggle}^{\rm max}$ at low switching current. The 16.75-GHz divided-by-four output waveform for a 67-GHz input in the PT-SFD at a PT ratio of 0.41 and the switching current of 1.28 mA is shown in Fig. 10.

The dependence of the maximum operating frequency $f_{\rm toggle}^{\rm max}$ on $V_L^{\rm total}$ at the switching current $I_{\rm CS}$ of 1.28 mA is shown in Fig. 11. In the conventional SFD, $f_{\rm toggle}^{\rm max}$ monotonically in-

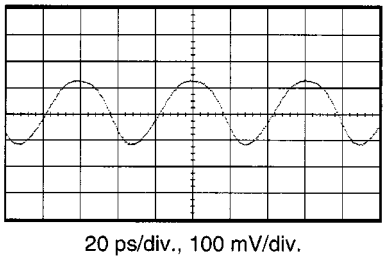

Fig. 10. 16.75-GHz divided-by-four output waveform of the PT-SFD for a 67-GHz clock input. PT ratio is 0.41, the switching current is 1.28 mA, and the total logic swing voltage is 250 mV.

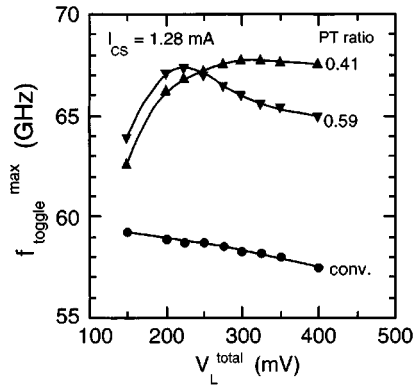

Fig. 11. Dependence of maximum operating frequencies $f_{\rm toggle}^{\rm max}$ on the total logic swing voltage $V_L^{\rm total}$ for the switching current $I_{\rm CS}$ of 1.28 mA.

creases as $V_L^{\rm total}$ reduces. On the contrary, in the PT-SFD, there was the optimum $V_L^{\rm total}$, which produces the highest $f_{\rm toggle}^{\rm max}$, depending on the PT ratio. The optimum values at PT ratios of 0.59 and 0.41 are approximately 225 and 325 mV, respectively. Thus, the latching voltage is about 130 mV.

The power consumption of the PT MS-TFF is 175 mW at a supply voltage of -5.2 V. This is about 1/5 that of a 66-GHz SFD with transferred-substrate InAlAs/InGaAs HBTs [1]. The high-speed low-power SFD operation demonstrates that this SiGe HBT technology (like high-reliability and cost-effectiveness Si technology) will play an important role in future millimeter-wave systems. A chip micrograph of the 1/4 PT-SFD, including an enlarged image of the PT MS-TFF region (taken after the first-metal formation) is shown in Fig. 12. The PT-SFD occupies a 0.97 $\times$ 1.1 mm area and the main circuit region takes up 450 $\times$ 100 μm. The PT MS-TFF takes up only 80 $\times$ 60 μm. All circuit elements (e.g., transistors, resistors, and even interconnects) are laid out symmetrically. The dc-bias terminals are connected via MIM capacitors to ensure a stable voltage supply.

V. Summary

A 67-GHz 1/4 PT-SFD using 0.2-μm self-aligned SEG SiGe HBTs, with a 122-GHz cutoff frequency, a 163-GHz maximum oscillation frequency, and an average ECL gate delay time of 5.65 ps, has been developed. The PT MS-TFF circuit of the divider increases the maximum operating frequency to about 15% higher than that of a conventional MS-TFF, yet the power consumption of the divider is 175 mW, which is 1/5 that of comparable dividers, at a supply voltage of -5.2 V. This excellent

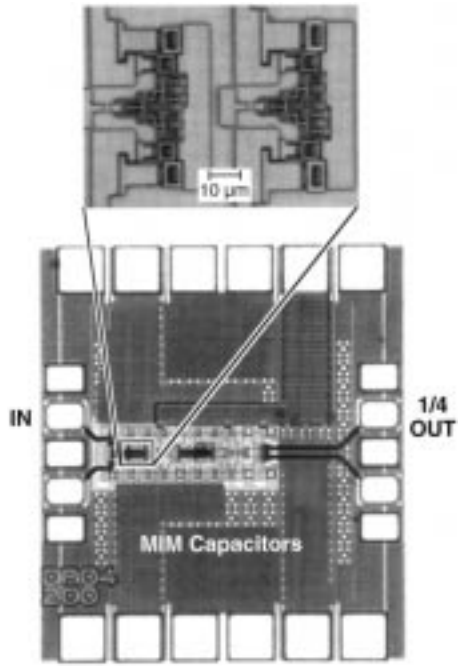

Fig. 12. Chip photomicrograph of the 1/4 PT-SFD, including an enlarged image of the PT MS-TFF region. The PT-SFD occupies a 0.97 × 1.1 mm area and the PT MS-TFF takes up only 80 × 60 μm.

performance shows that Si bipolar technology, which offers high reliability and cost effectiveness, will play a major role in future millimeter-wave systems.

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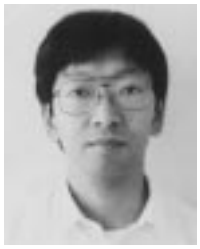

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